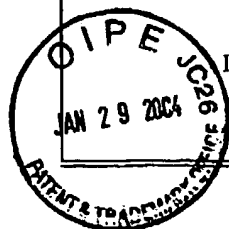| **FORM PTO-1449**	Atty. Docket No.: I69.12-0554	Application No.: 10/633,791
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	First Named Inventor: Erozan M. Kurtas	
	Filing Date: August 4, 2003	Group Art: ~~2631~~ 2133

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Examiner Initials		Document No.	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents
SWD	AA	6,112,326	09/29/2000	Khayrallah
	AB			
	AC			
	AD			

FOREIGN PATENT DOCUMENTS

		Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Translation Yes No
SWD	AE	EP 1 137 002 A1	09/26/2001	Miyauchi, Toshiyuki	
	AF				
	AG				

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

SWD	AH	William E. Ryan, Concatenated Codes for Class IV Partial Response, IEEE Transactions On Communications, Vol. 49., No. 3, March 2001, pp. 445-454.
SWD	AI	Joachim Hagenauer, Iterative Decoding of Binary Block and Convolutional Codes, IEEE Transactions On Information Theory, Vol. 42, No. 2, March 1996, pp. 429-445.
SWD	AJ	D. Divsalar and F. Pollara, Multiple Turbo Codes for Deep-Space Communications, TDA Progress Report 42-121, May 15, 1995, pp. 66-77
SWD	AK	Tom V. Souvignier, Turbo Decoding for Partial Response Channels, IEEE Transactions On Communications, Vol. 48, No. 8, August 2000, pp. 1297-1307.

EXAMINER:	DATE CONSIDERED: 9/14/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449		Atty. Docket No.: 169.12-0554	Application No.:
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		First Named Inventor: Erozan M. Kurtas et al.	
		Filing Date: Herewith	Group Art: 2133

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Name	Class	Sub Class	Filing Date If Appropriate
SWB	AA	5,812,601	09/22/98	Schramm	375	262	11/15/96
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SWB	AC	"Reduced Complexity In-Phase/Quadrature-Phase Turbo Equalisation Using Iterative Channel Estimation", B.L. Yeap, et al., *0-7803-7097-1/01 IEEE*, 2001.
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SWB	AF	"VLSI Architectures for Turbo Codes", Guido Masera, et al., *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS,* Vol. 7, No. 3, September 1999.
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SWB	AM	"A Soft-Input Soft-Output APP Module for Iterative Decoding of Concatenated Codes", S. Benedetto, et al., *IEEE COMMUNICATIONS LETTERS, Vol. 1, No. 1,* January 1997.

EXAMINER: _____ DATE CONSIDERED: 9/19/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.